SPECIFICATION AMENDMENTS:

Please amend the paragraph bridging pages 8 and 9 of the Specification to read as follows:

The present invention further provides a liquid crystal apparatus, comprising:

a liquid crystal device comprising an active matrix substrate having thereon a plurality of signal lines arranged [[in]] in columns, a plurality of scanning lines in arranged rows, and pixel electrodes each

connected via a pixel switch to an intersection of the signal lines and the scanning lines so as to supply picture signals to the pixel electrodes via the signal lines, a counter substrate disposed opposite to the active matrix substrate, and a liquid crystal disposed between the active matrix substrate and the counter substrate, and

drive means for driving the liquid crystal devices, wherein said drive means including:

a first common signal line and a second common signal line for supplying the picture signals,

picture signal-supplying means for supplying picture signals of one polarity to the first common signal line and picture signals of the other polarity to the second common signal line,

a first and a second transfer switch provided to each column signal line for selectively supplying one of picture signals supplied to the first and second common signal lines to each column signal line, and

dot inversion drive means for:

in a first frame, selectively turning on the first transfer switches for odd-numbered column signal lines and the second transfer switches for even-numbered column signal lines at the time of scanning odd-numbered scanning lines, and selectively turning on the second transfer switches for odd-numbered column signal lines and the first transfer switches for even-numbered column signal lines at the time of scanning even-numbered scanning lines; and

in a second frame, selectively turning on the second transfer switches for odd-numbered column signal lines and the first transfer switches for even-numbered column signal lines at the time of scanning odd-numbered scanning lines, and selectively turning on the first transfer switches for odd-numbered column signal lines and the second transfer switches for even-numbered column signal lines at the time of scanning even-numbered scanning lines.

Please amend the paragraph bridging pages 13 and 14 of the Specification to read as follows:

Now, the operation of the electronic circuit shown in Figure 1 is described. First, digital data of identical level (e.g., binary-coded 8 bit data of (00111100)) is [[are]]supplied to the respective data latch circuits 2 and to a latch circuit 2A in the leftmost offset data generating circuit, where the digital data is latched in synchronism with the latch clock signal (LATCH CLK). At this time, the memory circuits 3, controlled by clock signals (MEMO_CLK), for memorizing respective offset correction data (e.g., of 5 bits) are reset to a prescribed level (e.g., 5 bit data of (10000) as a default). As a result, the respective D/A converters 1 are supplied

with digital signals of an identical level, but analog outputs of the respective D/A converters 1 include superposed offset values peculiar to the respective D/A converters 1, so that the analog outputs can be respectively different. Now, switches 9 connected to the D/A converters 1 are sequentially turned on. Then, the analog outputs of the respective D/A converters 1 are compared with the analog output of the D/A converter lA in the offset correction data-generating D/A converter circuit to measure respective offset values contained in the analog outputs of the respective D/A converters 1 relative to the D/A converter 1A. The measured offset values are sequentially written in the respective memory circuits 3 for the respective D/A converters 1 by the encoder circuit 6.

Please amend the paragraph bridging pages 14 and 15 of the Specification to read as follows:

Figure 2 is a block diagram of a liquid crystal display apparatus including the electronic circuit of Figure 1. Referring to Figure 2, the analog outputs of each D/A converter 1 are supplied to vertical signal lines 7 via signal transfer switches 19 and then to respective pixels 8. Each pixel 8 comprises a pixel transistor, an additional capacitance and a liquid crystal. Scanning lines 11 are sequentially selected depending on an output of a vertical shift register (VSR) 12 to turn on the pixel transistors on each selected scanning line, thereby supplying picture signals (outputs) from the D/A converters 1 to the respective pixels. The above-mentioned offset correction operation may be performed at the time of initial power supply, more preferably at a blanking period for each field operation.